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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/945,309	KIRK, STEVE VAN	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) *31-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☒ Interview Summary (PTO-413) Paper No(s). 6 .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-30, drawn to an apparatus for a semiconductor die, including a substrate, an integrated circuit and a measurement circuit both supported by the substrate, classified in class 714, subclass 724.

II. Claims 31-44, drawn to a method of forming an integrated circuit and a measurement circuit both supported by the substrate, classified in class 438, subclass 15.

III. Claims 45-49, drawn to a method of measuring a ground bounce voltage value of an integrated circuit on a substrate and using a measurement circuit on the substrate, which includes a data acquisition system, classified in class 324, subclass 765.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the process (Invention II) can be used to form any typical TTL Integrated Circuit semiconductor device on a printed circuit board, other than a memory circuit supported by a substrate. Also, the product (Invention I) can be

made using materially different process, such as, a non-conductive layer on a circuit board for forming the integrated circuit package on the circuit board.

Inventions I and III are related as product and process of use. The inventions can be shown to be distinct if either or both of the following can be shown: (1) the process for using the product as claimed can be practiced with another materially different product or (2) the product as claimed can be used in a materially different process of using that product (MPEP § 806.05(h)). In the instant case the process (invention III) for using the product (invention I) can be practiced with another materially different product, such as testing any typical TTL Integrated Circuit on a printed circuit board.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

The examiner has required restriction between product and process claims. Where applicant elects claims directed to the product, and a product claim is subsequently found allowable, withdrawn process claims that depend from or otherwise include all the limitations of the allowable product claim will be rejoined in accordance with the provisions of MPEP § 821.04. **Process claims that depend from or otherwise include all the limitations of the patentable product** will be entered as a matter of right if the amendment is presented prior to final rejection or allowance, whichever is earlier. Amendments submitted after final rejection are governed by 37 CFR 1.116; amendments submitted after allowance are governed by 37 CFR 1.312.

In the event of rejoinder, the requirement for restriction between the product claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to

be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103, and 112. Until an elected product claim is found allowable, an otherwise proper restriction requirement between product claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowed product claim will not be rejoined. See "Guidance on Treatment of Product and Process Claims in light of In re Ochiai, In re Brouwer and 35 U.S.C. § 103(b)," 1184 O.G. 86 (March 26, 1996). Additionally, in order to retain the right to rejoinder in accordance with the above policy, Applicant is advised that the process claims should be amended during prosecution either to maintain dependency on the product claims or to otherwise include the limitations of the product claims. **Failure to do so may result in a loss of the right to rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

During a telephone conversation with Edward J. Brooks, III on December 10, 2003 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-30. Affirmation of this election must be made by applicant in replying to this Office action. Claims 31-49 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-7, 9, 12,14, 16-21, 23-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Haulin (US 5498972).

Regarding Claim 1, Haulin discloses an apparatus and method for monitoring the supply voltage and ground connections on an integrated circuit (IC), comprising:

A substrate (3, Figure 1), an integrated circuit (11, Figure 3) supported by the substrate, wherein the integrated circuit includes a test domain having a test voltage (VCC) and a reference domain having a reference voltage (GND), which are connected to voltage supply pin 25 and ground connection pin 27 at the integrated circuit (11, Figure 3), which in turn are connected to voltage supply plane 19 (VCC) and ground plane 21 (GND) of substrate 3, in Figure 2.

And a measurement circuit (voltage monitor module, 31) supported by the substrate, wherein the measurement circuit monitors the test voltage (VCC) and a reference voltage (GND) for measuring the difference across VCC and GND, Figure 5.

Regarding Claim 3, according to Haulin, the integrated circuit (11) includes a switching logic circuit (control logic 37, Figure 3) connected to the test domain.

Regarding Claims 4, 5, 17, 19, 23, 25, 28, the measurement circuit (41) includes a peak detector (41) and a comparison circuit (45).

Regarding Claim 6, 18, 24, 27, 29, Haulin discloses the common limitation as recited in claim 1 above and in addition he discloses a measurement circuit (41), which

includes a peak detector (41) and a comparison circuit (45), which is functionally equivalent to analog-to-digital converter (A/D), since the input to the measurement circuit is analog signal and the output is converted to a digital signal.

Regarding Claim 7, Haulin discloses the common limitation as recited in claim 1 above and in addition he discloses a plurality of leads between (control logic 37 and pins 39) on the substrate and electrically connected to the plurality of leads by a plurality of wire bonds for connecting pins 39, Figure 3.

Regarding Claim 9, 14, according to Haulin, the integrated circuit (11) includes a processor, such as a measurement circuit (412) including a peak detector (41) and a comparison circuit (45), which is connected to the test domain having a test voltage (VCC).

Regarding Claim 12, Haulin discloses the common limitation as recited in claim 1 above, and in addition he discloses a conductive layer (conductive path 15) connected to the plurality of leads on IC, Figure 1 and where the plurality of leads are connected by a plurality of wire bonds, Figure 3.

Regarding Claims 16, 20, Haulin discloses the common limitations as recited in claim 1 and 7 above. In addition he discloses a circuit board (3) having a conductive layer 15, Figure 1. Further, he discloses at least two integrated circuit packages, which may be a first memory integrated circuit package and a second memory integrated circuit package (11) connected to the conductive layer (15), having memory bus, which is shown in detail in Figure 3. The limitations of integrated circuit package (11) were described previously in claims 1 and 7, above.

Regarding Claim 21, 26, Haulin discloses the common limitation as recited in claim 1 above, and in addition he discloses a measurement circuit including data acquisition system (41) comprising a peak detector (41) and a comparison circuit (45).

Regarding Claim 30, with respect to the plurality of differences from the data acquisition system, such as the test results from the output of the comparator (45), Haulin discloses boundary scan cell 36, which can be used by a computer terminal, as a means of reading the test result, Figure 5. It is described in the above-mentioned publication IEEE Standard B1149.1 IEEE Standard Test Access Port and Boundary-Scan Architecture (column 8, line 39-42).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 11, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haulin (US 5498972).

Regarding Claims 10, 11, 15, Haulin does not explicitly include a memory array with an output driver connected to the test domain. However, he discloses recording means such as (memory 8, Figure 1) connected to the integrated circuit (11) for storing

test results. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate recording means such as a memory with driving circuit capability, for recording the results of the testing operation, since on board memory provides high speed storage access.

Claims 2, 8, 13, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haulin (US 5498972) in view of Roy et al. (US 6195613).

Regarding Claim 2, 8, 13, 22, Haulin does not explicitly specify that the test domain is a first ground connection of the integrated circuit. However, Haulin, as indicated above, he discloses test voltage potential (VCC) corresponding to the test domain and a reference voltage (GND) corresponding to the reference domain, which is defined as second ground potential of the integrated circuit.

Furthermore, Roy et al. (US 6195613) discloses power distribution system, 100, Figure 1, comprising a pair of square conductive planes 110 and 120, such 110 corresponding to a first ground connection and 120 corresponding to a second ground connection. The voltage 130 represents the difference between the first and second ground.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to connect a pair of square conductive planes (110 and 120), corresponding to a first and a second ground connection, respectively, as taught by Roy, across the measurement circuit (voltage monitor module) of Haulin, for the

purpose of measuring the difference between two ground planes, thereby reducing the ground bounce by using continuous ground and power supply planes in parallel, which act as "bypass" capacitor for reducing the power supply droop, thus resulting in a more reliable ground differential measurement.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4900.

James C Kerveros
Examiner
Art Unit 2133

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By: 12/12/03

Date: 12 December 2003
File: Non-Final Rejection

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